

Curriculum Vitae: Tommaso Cucinotta

Personal data

Birth date and place: April'74, Potenza (Italy) LinkedIn Profile: [tommasocucinotta](#)
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Current status

Dec 2015 to date: *Associate Professor* at the Real-Time Systems Laboratory (ReTiS) of Scuola Superiore Sant'Anna

July 2019 to date: *Coordinator* of the Cyber-Physical Research Area of Scuola Superiore Sant'Anna

RESEARCH TOPICS & COMPETENCIES

- Real-time and reliable NoSQL Data Stores for Cloud services
- Adaptive resource management and scheduling in Cloud Computing & Network Function Virtualization infrastructures
- Artificial Intelligence and Machine Learning to support Data Center Operations in Cloud & NFV infrastructures
- Platforms for real-time data streaming and analytics
- Quality of service control for adaptive soft real-time applications, including multimedia and IMS systems
- Operating Systems for real-time and embedded applications, and many-core and massively distributed systems
- Trusted computing and confidentiality in Cloud Computing
- Smart-cards: interoperability, protocols and architectures
- Digital signatures, biometrics identification, multicast security

Experience highlights (details below)

- 10 Granted and 19 Filed EU and US Patents** in the areas of security, resource management and scheduling
- 38 International Journal Publications**, including [IEEE Transaction on Computers](#), [IEEE Transaction on Cloud Computing](#), [IEEE Transaction on Industrial Informatics](#), and [ACM Transactions on Embedded Computing Systems](#)
- 112 International Conference and Workshop Peer-reviewed Publications and 14 Book Chapters**
- 3 EU Projects scientific responsibility** (overall, raised and managed funds for ~900K EUR), made significant contributions to **8 EU Projects** and other national research projects
- General or program co-chair** of 16 international conferences or workshops
- Guest editor** of 5 special issues of international journals; reviewed several papers for international journals
- Program committee member** of more than 40 international conferences and workshops
- Mentored** 9 PhD students, 13 under-graduate students for their MSc thesis and 3 Bell Labs interns
- >40 teaching assignments**
- 2 years Software Engineer in AWS**, improving performance and scalability of **DynamoDB**
- 5 consultancy assignments by external companies for production-quality software (in the areas of embedded systems, multimedia applications and Linux kernel)
- 14 open-source projects** created and/or contributed to
- Long-standing experience in low-level programming since age of 12, including: development of 100% Assembler applications (text, image, music editors, demos on Commodore 64 and Amiga 500) with direct access to hardware and interrupt registers; writing of malwares propagating through disk boot sector infection; hacking into object code of Windows applications for breaking license verification code

AWARDS AND RECOGNITIONS

- May 2024:** [Best Paper Award](#) for co-authored paper at RAGE 2024
- Apr 2021:** [Best Student Paper Award](#) for co-authored paper at CLOSER 2021
- May 2020:** [Best Paper Award](#) for co-authored paper at CLOSER 2020
- Feb 2020:** [Best Paper Award](#) for co-authored paper at ICN 2020
- Mar 2019:** [Best Paper Award](#) for co-authored paper at ICN 2019
- Apr 2018:** [Best Paper Award](#) for co-authored paper at ICN 2018
- Apr 2014:** Selected as [featured researcher profile](#) in highlight on the Bell Labs website
- Jul 2018:** Eligibility as full professor in Computer Engineering (Abilitazione Scientifica Nazionale da professore di I Fascia nel SC 09/H1 – SSD ING-INF/05)

- **Nov 2020:** Eligibility as full professor in Computer Science (Abilitazione Scientifica Nazionale da professore di I Fascia nel SC 01/B1 – SSD INF/01)
- **Oct 2013:** [IEEE Senior Member grade](#) elevation
- **Dec 2010:** [Best-paper award](#) for co-authored paper at IEEE SOCA 2010

PhD Board Membership

- **a.y. 2021/22, 2022/23, 2023/24, 2024/25:** **Board Member** of the National PhD in Artificial Intelligence – AI & Society branch at Scuola Superiore Sant’Anna, jointly offered with University of Pisa, Politecnico di Torino, National Research Council and others
- **a.y. 2017/18, 2018/19, 2019/20, 2020/21:** **Board Member** of the PhD in Data Science, joint program at Scuola Superiore Sant’Anna, Scuola Normale Superiore, University of Pisa, National Research Council and Scuola IMT Lucca
- **a.y. 2016/17, 2022/23, 2023/24, 2024/25:** **Board Member** of the PhD in Emerging Digital Technologies at Scuola Superiore Sant’Anna

Organization of international peer-reviewed events and editorial roles in peer-reviewed international journals

- **Associate Editor** for [IEEE Transactions on Services Computing](#), Oct 2023 to date
- **General Co-Chair** of the 6th International Workshop on Power Management and Scheduling in the Linux Kernel (OSPM Summit), May 31-31 2024, Toulouse (France)
- **Guest Editor** of the Special Issue on Virtualization in High-Performance Cloud Computing of the Elsevier Journal of Systems Architecture (JSA), 2023
- **General Co-Chair** of the 18th International Workshop on Virtualization in High-Performance Cloud Computing (VHPC 2023), May 25th 2023, Hamburg, Germany, co-located with ISC-HighPerformance 2023
- **General Co-Chair** of the 5th International Workshop on Power Management and Scheduling in the Linux Kernel (OSPM Summit), Apr 17-19 2023, Ancona (Italy)
- **General Co-Chair** of the 17th International Workshop on Virtualization in High-Performance Cloud Computing (VHPC 2022), June 2nd 2022, Hamburg, Germany, co-located with ISC-HighPerformance 2022
- **Guest Editor** of the Special Issue on the 2020 IEEE Symposium on Real-time Distributed Computing (ISORC 20) of the Elsevier Journal of Systems Architecture (JSA), 2022
- **Program Co-Chair** of the 23rd IEEE International Symposium on Real-Time Distributed Computing (ISORC 2020), May 12-14 2019, Nashville, USA
- **General Co-Chair** of the 4th International Workshop on Power Management and Scheduling in the Linux Kernel (OSPM Summit), May 11-13 2020, Pisa (Italy)
- **General Co-Chair** of the 3rd International Workshop on Power Management and Scheduling in the Linux Kernel (OSPM Summit), May 20-22 2020, Pisa (Italy)
- **General Co-Chair** of the 2nd International Workshop on Power Management and Scheduling in the Linux Kernel (OSPM Summit), April 16-18 2018, Pisa (Italy)
- **General Co-Chair** of the 1st International Workshop on Power Management and Scheduling in the Linux Kernel (OSPM Summit), April 3-4 2017, Pisa (Italy)
- **General Co-Chair** of the 9th International Workshop on Virtualization in High-Performance Cloud Computing (VHPC 2014), August 25-29 2014, Porto, Portugal, co-located with Euro-Par 2014
- **General Co-Chair** of the 2nd International Workshop on Real-Time and Distributed Computing in Emerging Applications (REACTION 2013), December 2013, Vancouver, Canada, co-located with IEEE RTSS 2013
- **Guest Editor** of the Special Issue on Real-time and distributed computing in emerging applications (REACTION) of the Elsevier Journal of Systems Architecture (JSA), Vol. 61, Issue 5-6, May 2015
- **General Co-Chair** of the 4th International Workshop on Analysis Tools and Methodologies for Embedded and Real-time Systems (WATERS 2013), July 2013, Paris, France, co-located with ECRTS 2013
- **General Co-Chair** of the International Workshop on Real-Time and Distributed Computing in Emerging Applications (REACTION 2012), December 2012, San Juan, Puerto Rico, co-located with IEEE RTSS 2012
- **General Co-Chair** of the 3rd International Workshop on Analysis Tools and Methodologies for Embedded and Real-time Systems (WATERS 2012), July 2012, Pisa, Italy, co-located with ECRTS 2012
- **Guest Editor** of two Special Issues on Analysis Tools and Methodologies for Embedded and Real-time Systems (WATERS) of the Elsevier Journal of Systems Architecture (JSA), 2012-2014

- ❑ **General Co-Chair** of the 2nd International Workshop on Analysis Tools and Methodologies for Embedded and Real-time Systems (WATERS 2011), July 2011, Porto, Portugal, co-located with ECRTS 2011
- ❑ **Program Co-Chair** of the Fourth IEEE International Workshop on Real-Time Service-Oriented Architecture and Applications (RTSOAA 2011), December 2011, Irvine, CA, co-located with IEEE SOCA 2011.
- ❑ **General Co-Chair** of the 1st International Workshop on Analysis Tools and Methodologies for Embedded and Real-time Systems (WATERS 2010), July 2010, Brussels, Belgium, co-located with ECRTS 2010

Research grants

- ❑ **Jan 2020 – Dec 2022: Head** of the research unit at Scuola Superiore Sant'Anna within the AMPERE European Project (H2020 ICT 871669)
- ❑ **Feb 2008 – Feb 2011: Head** of the research unit at Scuola Superiore Sant'Anna within the IRMOS European Project (FP7 ICT 214777)
- ❑ **Feb 2010 – Jan 2012: Head** of the research unit at Scuola Superiore Sant'Anna within the S(o)OS European Project (FP7 FET 248465)

Peer-review for international journals, conferences, and workshops

- ❑ **Review Committee Member** for the 2014 EuroSys Roger Needham PhD Award
- ❑ **Program Committee member** of ACM EdgeSys 2023, SC 2022, IEEE IC2E 2021-2023, IEEE SDN-NFV 2020, IEEE RTAS 2018, 2017, 2013 and 2012, IEEE ICPS 2018, IEEE INDIN 2018, CLOSER 2020, 2019, 2014 and 2013, IEEE ETFA 2021-2019, 2017 and 2012, IEEE SIES 2013
- ❑ **Program Committee member** of MobileServerless 2021, VHPC 2021-2018 and 2010-2012, IEEE SOCNE 2017, 2012 and 2011, EwiLi 2017, ACM CF 2017, REACTION 2017, SeaClouds 2014, RTLWS 2012, OPODIS 2011, IEEE/IFIP EUC 2011, IEEE ICSS 2011, CLOSER 2011-2013, CSPNA 2011, IEEE SOCA 2010-2012, SOMRES 2011, the Workshop on trends, issues and challenges in future high-end computing, AHM 2010, CDC, DATE
- ❑ **Reviewer** for: IEEE Transactions on Computers, on Automatic Control, on Cloud Computing, on Industrial Informatics, on Parallel and Distributed Systems, on Mobile Computing; Springer Journal on Real-Time Systems, on Service Oriented Computing and Applications; Wiley Software Practice & Experience; Elsevier Journal on Systems and Software, on System Architecture, on Computer and Systems, on Parallel and Distributed Computing.

Professional experience

- ❑ **Jul 2014 to Feb 2016:** Senior Software Development Engineer at **Amazon DataBase Services**, Dublin (Ireland), working on aspects related to the real-time performance of AWS DynamoDB.
- ❑ **Jan 2012 – Jun 2014:** Researcher (Member of Technical Staff) at Bell Labs, Alcatel-Lucent, Dublin (Ireland).
- ❑ **Oct 2011 – Jan 2012:** Research Associate at the Real-Time Systems Laboratory (RETIS) of Scuola Superiore Sant'Anna (SSSA), Pisa (Italy).
- ❑ **Oct 2005 – Sep 2011:** Assistant Professor at the Real-Time Systems Laboratory (RETIS) of Scuola Superiore Sant'Anna (SSSA), Pisa (Italy).
- ❑ **Feb 2009:** Consultant for Evidence s.r.l., Pisa: development of a G.729 codec for a VoIP gateway – in production
- ❑ **Nov 2008 – Jan 2009:** Collaboration for the design and realization of a security mechanism for distributed control applications, European Project CHAT INFISO-ICT-224428 , University of Trento, Italy.
- ❑ **Jan 2008:** Collaboration within the European Project INTEREST IST-33661, Evidence s.r.l., Pisa (Italy).
- ❑ **Oct 2007:** Collaboration for “Development of the RT-Druid tool”, Evidence s.r.l., Pisa (Italy).
- ❑ **Jan 2007:** Collaboration for the “Requirements analysis of the RT-Druid tool”, Evidence s.r.l., Pisa (Italy).
- ❑ **Oct 2004 – Jan 2005:** Collaboration within the OCERA FP5 European Research Project IST-2001-35102, SSSA.
- ❑ **May – Aug 2005:** Collaboration on “Performance analysis techniques for control systems with computing resources constraints”, European Project RECSYS IST-2001-37170, SSSA.
- ❑ **Feb – Mar 2005:** Collaboration within the OCERA FP5 European Research Project IST-2001-35102, SSSA.
- ❑ **May – Jun 2004:** Collaboration on Experimentation on Embedded platforms for Multimedia Applications, SSSA.
- ❑ **Jan – Apr 2004:** Collaboration to the activities of the FABRIC Research Project IST-2001-37167, SSSA.
- ❑ **Jul – Dec 2003:** Collaboration to the activities of the European Research Project ARTIST IST-2001-34820, SSSA.
- ❑ **Jun – Jul 2003:** Collaboration for using digital signatures in internal processes, Link Research Project, SSSA.

- ❑ **Jul – Aug 2002:** Collaboration on “Support for experimenting with digital signatures in the internal processes”, Project Link “Piano di Potenziamento della Rete di Ricerca e di Sviluppo nel Territorio”, SSSA.
- ❑ **Oct 2001:** Technological evaluation of an investment proposal within the “Startech Sviluppo Italia” Program, on the issue of verifying printed digital signatures, Technodeal s.r.l., Pisa (Italy).
- ❑ **Aug – Oct 2001:** *Internship in SCHLUMBERGER SMART CARDS, AUSTIN (TX):* Design and implementation of an open-source middleware for smart cards. Software currently available in most Linux distributions.
- ❑ **Jan – Jun 2001:** Design of an advanced document object model for a *digital library* and implementation within the *Dienst* software by means of the *OLP Protocol*. Project developed in collaboration with “Consorzio Nazionale delle Ricerche, Istituto di Elaborazione dell'Informazione / CNR-IEI”.
- ❑ **Mar – Apr 2001:** Design and realization of a web-based *content management framework* for sharing digital documents. Implemented within the *Zope* application server. Currently online at <http://link.sssup.it>.
- ❑ **Jul – Sep 2001:** Design of a web-based *Electronic Registry System* compliant with the Italian national laws and implementation within the *Zope application server*. Project committed to SSSA by the Authority for Information Technologies in Public Administrations (AIPA).
- ❑ **Jul – Dec 2000:** Realization of a software tool for digital signatures, within the “Project for electronic document security and digital signatures”, SSSA.

PhD and MSc students I acted as supervisor, examiner, or defense opponent for

- ❑ **Sep 2019 to date:** supervisor of Gabriele Ara for his PhD in Emerging Digital Technologies at Scuola Sant’Anna, focusing on power-aware real-time scheduling on heterogeneous platforms
- ❑ **Sep 2018 to date:** supervisor of Agostino Mascitti for his PhD in Emerging Digital Technologies at Scuola Sant’Anna, focusing on power-aware real-time scheduling on heterogeneous platforms
- ❑ **2017 to date:** co-supervisor of Daniel Bristot de Oliveira for his joint PhD at Scuola Sant’Anna and Universidad Federal de Santa Caterina, focusing on automata-based run-time verification of the Linux kernel
- ❑ **Sep 2017 – Feb 2018:** supervisor of Francesco de Gioia for a MSc thesis at University of Pisa, focusing on “testing in development tool-chains for RISC-V architectures,” carried out as an internship at Gaisler Research (Sweden)
- ❑ **Jul 2017 to 2018:** supervisor of Alessio Balsini for his PhD in Emerging Digital Technologies at Scuola Sant’Anna, focusing on heterogeneous and power-aware real-time scheduling in the Linux kernel
- ❑ **Nov 2016 to 2017:** supervisor of Federico Civerchia in his PhD in Emerging Digital Technologies at Scuola Sant’Anna, focusing on Internet of Things
- ❑ **Mar – Jun 2014:** supervisor of Andrea Meroni during his internship at Bell Labs Ireland about “On-Demand State Migration Protocol for Elastic IMS Cloud Components”, work submitted as MSc thesis at University of Pavia (Italy)
- ❑ **2010-2016:** co-tutor of Juri Lelli for the PhD in Computer Engineering about “Multiprocessor Real-Time Scheduling on General Purpose Operating Systems” at Scuola Superiore Sant’Anna, Pisa (Italy)
- ❑ **Feb – May 2013:** supervisor of Aram Santogidis during his internship at Bell Labs Ireland about “Simulation of Real-Time Cloud Computing Applications”
- ❑ **Jul – Sep 2012:** supervisor of Nilo Redini during his intership at Bell Labs Ireland about “Access control models for a novel Internet-scale file-system”, project submitted as MSc thesis at University of Pisa (Italy)
- ❑ **Jun 2012:** external opponent of Mikael Åsberg for the licensiate thesis defense in Comp. Science and Engineering on “Development of Hierarchical Real-Time Systems” at the Mälardalen University, Västerås (Sweden)
- ❑ **2006-2010:** co-tutor of Fabio Checconi for the PhD in Computer Engineering on “Proportional Share Scheduling in General Purpose Operating Systems: Theory and Practice” at Scuola Superiore Sant’Anna, Pisa (Italy)
- ❑ **2008-2011:** supervisor of Gaetano Anastasi for the PhD in Computer Engineering focusing on “Quality of Service Management in Service Oriented Architectures” at Scuola Superiore Sant’Anna, Pisa (Italy)
- ❑ **2011:** external examiner for the Degree of Master of Information Systems and Technology by Research of Zhe Sun, with a thesis on “Research on a New Peer to Cloud and Peer Model and a Deduplication Storage System” at the University of Wollongong
- ❑ **2010:** supervisor of Giacomo Bagnoli for the MSc thesis in Computer Engineering on “Design and development of a mechanism for low-latency real time audio processing on Linux” at the University of Pisa (Italy)
- ❑ **2009:** supervisor of Andrea Angella for the MSc thesis in Computer Engineering on “SCOTT: un’architettura modulare per il testing di soluzioni basate su smartcard ” at the University of Pisa (Italy)
- ❑ **2009:** supervisor of Emanuele Gringeri for the MSc thesis in Computer Engineering on “Improving security and memory management in the MUSCLE card framework ” at the University of Pisa (Italy)

- **2008:** supervisor of Alberto Donadoni for the MSc thesis in Computer Engineering on “Progetto e realizzazione di un'architettura software modulare ed estendibile per il monitoraggio e la gestione dei parametri di esecuzione di applicazioni soft real-time” at the University of Pisa (Italy)
- **2006:** supervisor of Riccardo Bresciani for the BSc thesis in Computer Engineering on “Crittografia a Curve Ellittiche su FPGA Altera Cyclone II” at the Scuola Superiore Sant'Anna, Pisa (Italy)
- **2003:** supervisor of Alessandro Pieroni for the MSc thesis in Computer Engineering on “Realizzazione di un'API crittografica per smart-card in Java” at the University of Pisa (Italy)
- **2003-2004:** co-tutor of Riccardo Brigo for the PhD in Computer Engineering on Fingerprint Matching on Programmable Smart-Cards at Scuola Superiore Sant'Anna, Pisa (Italy)
- **2002:** supervisor of Riccardo Brigo for the MSc thesis in Computer Engineering on “Sviluppo di un sistema di protezione per smart-card basato su algoritmi di verifica biometrica on-board” at the University of Pisa
- **2002:** supervisor of Paolo Grimaccia and Matteo Ferrari for the MSc thesis in Computer Engineering on “Progetto e realizzazione di un emulatore Java Card” at the University of Pisa (Italy)

Teaching experience

- **Yearly, from a.y. 2016/17 to date:** Courses on “Cloud Computing and Big-Data” and “Cloud Computing and Big-Data Lab” in the PhD in Emerging Digital Technologies at Scuola Superiore Sant'Anna, the PhD in Data Science at Scuola Normale Superiore of Pisa, and the Nation-wide International PhD in Artificial Intelligence at University of Pisa
- **a.y. 2021/22:** Real-Time and High-Performance Computing on Linux, PhD in Emerging Digital Technologies at Scuola Superiore Sant'Anna
- **a.y. 2021/22:** Java Programming Fundamentals, Course for Honor Students at Scuola Superiore Sant'Anna
- **a.y. 2020/21:** Computer Security, Course for Honor Students at Scuola Superiore Sant'Anna
- **a.y. 2020/21:** Advanced Java Programming, Course for Honor Students at Scuola Superiore Sant'Anna
- **a.y. 2020/21:** C/C++ Programming Foundations, Course for Honor Students at Scuola Superiore Sant'Anna
- **Yearly, from a.y. 2016/17 to 2019/20:** Course on “Component-Based Software Design,” MSc degree in Embedded Computing Systems jointly organized by Scuola Sant'Anna and University of Pisa. Course language: English
- **March 2016:** Course “From Classical Distributed Systems to Cloud Computing” - external lecturer for PhD students at the Computer Engineering Dept. of University of Pisa. Course Language: English
- **Yearly, from 2006 to 2011:** Course on “Design of Embedded System”, Faculty of Engineering, University of Siena
- **Yearly, from 2002 to 2011:** International Master on Information Technology and Software Engineering – Module “*System Security and Cryptography*”, SSSA. Course language: English.
- **Yearly, from 2006 to 2011:** International Master on Communication Networks Engineering – Module “*System Security and Cryptography*”, SSSA. Course language: English.
- **Jun 2008:** Course on “Real-time operating systems”, SSSA “UNI-NORGE Project”, Ericsson, Rome.
- **Jun 2006:** Lecture on “Digital Signatures: *technological and juridical framework*”, Specialization course “*Codice dell'Amministrazione Digitale D. Lgs. n.82/2005*”, LiderLab, SSSA.
- **Mar 2006:** Lecture on “Technologies for e-Health Security”, Master on European Procurement and Transplantation Programs Management, SSSA
- **Nov 2005:** Lecture on “Informatics Basics”, Master on Innovation Management, SSSA
- **Oct – Nov 2005:** International Master on Information Technology and Communication Networks Engineering – Module “Java”, SSSA. Course language: English
- **Oct 2005 – Sep 2006:** Course on Industrial Informatics, Faculty of Engineering, University of Siena.
- **Oct – Dec 2005:** Professor assistant for a course on “Java Programming”, Faculty of Engineering, Pisa University.
- **Oct – Nov 2005:** Course on “Computer Architectures I”, Faculty of Engineering, University of Siena.
- **Oct 2005:** Specialization course “*Codice dell'Amministrazione Digitale D. Lgs. n.82/2005*” -- Lecture on “*Digital Signature: a technological viewpoint*”, LiderLab, SSSA.
- **May – Jul 2005:** Course on Industrial Informatics, Faculty of Engineering, University of Siena.
- **Apr 2004:** Course on “*e-commerce: technological issues related to authentication, security and privacy*” within the 2004 Edition of the Specialization Course “*Marketing e Distribuzione di Prodotti Assicurativi*”, SSSA.
- **Oct – Dec 2004:** Professor assistant for a course on “Informatics”, Faculty of Engineering, Pisa University.
- **Feb – May 2004:** Professor assistant for a course on “Informatics”, Faculty of Engineering, Pisa University.
- **Apr – May 2001:** Specialization course “*The Electronic Registry: specialistic knowledge for experts*”, SSSA.

- **May 2001:** Seminar “Technologies for innovating the Public Administration – Technologies and tools for ICT security”, SSSA.

Education

- **Jan 2001 – Jul 2004:** PhD in Computer Engineering, Scuola Superiore Sant'Anna University, Pisa (Italy), with *maximum marks* (“100/100 *summa cum laude*”). PhD research title: “Workflow and digital signature systems for Public Administration and enterprises”.
- **Sep 1992 – May 2000:** Master Degree in Computer Engineering (“Laurea in Ingegneria Informatica”), University of Pisa (Italy) with *maximum marks* (“110/110 *summa cum laude*”).
- **Sep 1988 – Jun 1992:** Senior High School specializing in Science Education.

POST-DEGREE STUDIES

- **June 2004 – May 2005:** **Research assistant** at the Real-Time Systems Laboratory (RETIS) of SSSA, for research activities in the European Project ARTIST
- **July 2001:** 13th International School for Computer Science Researchers “Foundations of Wide Area Network Programming”, Lipari, Messina (Italy).
- **Aug 2001:** Course on “Technologies and Innovation for improving the Public Administration internal processes”, modules “Digital signature systems” and “Organizational models for the PA innovations”, SSSA.
- **Nov 2002 – Jan 2003:** Course on “Management of internal innovation and external development processes” (with a module about “Team interaction and project management skills”), SSSA.

Patents

1. **T. Cucinotta**, M. Vannucci, A. Ritacco, G. Lanciano, A. Artale, J. Barata, E. Sposato. “A method of identifying and classifying the behavior modes of a plurality of data relative to a telephony infrastructure for Network Function Virtualization (*Metodo per identificare e classificare le modalità comportamentali di una pluralità di dati relativi ad un'infrastruttura telefonica per la network function virtualization*),” EU Patent **Grant** EP3772833B1 May 3rd 2023, (application IT102019000014241 August 7th 2019).
2. **T. Cucinotta**, M. Vannucci, A. Ritacco, G. Lanciano, A. Artale, J. Barata, E. Sposato. “A method of predicting the time course of a plurality of data relative to a telephony infrastructure for network function virtualization (*Metodo per predire l'evoluzione temporale di una pluralità di dati relativi ad un'infrastruttura telefonica per la network function virtualization*),” EU Patent **Grant** EP3772834B1 May 17th 2023, (application IT102019000014262 August 7th 2019).
3. **T. Cucinotta**, E. Jul. “Load-balancing and scaling of cloud resources by migrating a data session,” EU Patent **Grant** EP3046028B1, February 19th 2020 (application EP15305031 January 15th 2015).
4. **T. Cucinotta**. “Method of preventing access to sensitive data of a computing device,” US Patent **Grant** US10410004B2, Sep 10th, 2019 (application EP20130305396, March 28th, 2013).
5. E. Jul, **T. Cucinotta**, D. Cherubini. “Secure Data Processing,” EU Patent **Grant** EP2827276B1, July 3rd, 2019 (application EP20130306038, July 2013).
6. **T. Cucinotta**, S. Betgé-Brezetz. “Method and system for controlling the exchange of Privacy-Sensitive Information,” US Patent **Grant** US10237057B2, March 2019 (application EP20130360029, September 2013).
7. **T. Cucinotta**, M. Karnstedt. “Method for Performing Load Balancing, Distributed Computing Environment and Computer Program Product,” EU Patent **Grant** EP2940580B1, March 28th, 2018 (application EP20140305650, April 30th, 2014)
8. E. Jul, D. Cherubini, **T. Cucinotta**, D. Lugones. “Method for Balancing a Load, a System, an Elasticity Manager and a Computer Program Product,” US Patent **Grant** US9891941B2, February 2018 (application EP20140306301, October 2014).
9. **T. Cucinotta**, F. Chang, R. Viswanathan. “Exploiting Probabilistic Latency Expressions For Placing Cloud Applications,” US Patent **Grant** US9722930 B2, August 2017 (application 14/075727, November 2013).
10. **T. Cucinotta**, D. Cherubini, E. Jul. “Apparatus and method for secure data processing.” EU Patent **Grant** EP2672673B1, May 2016 (application 20120360045, June 2012).

FILED PATENTS

1. H. Gustafsson, L. Abeni, J. Eker, **T. Cucinotta**, R. Mini. "*Methods and Systems for Fault Mitigation with Additional State Transitions in Cloud Systems*," Filed Patent PCT/IB2023/057199, July 13th 2023
2. **T. Cucinotta**, M. Vannucci, G. Lanciano, F. Galli, F. Brau, A. Artale, E. Sposato, L. N. P. Jorge. "*Metodo per la gestione di risorse di un'infrastruttura per la network function virtualization*," Filed Patent IT10202000031034, December 16th 2020. Extensions:
3. **T. Cucinotta**, A. Derstepanians, M. Vannucci, A. Artale, S. Fichera, S. Lahiri, K. S. Avhad. "*Metodo per rilevare anomalie in un'infrastruttura per la network function virtualization*," Filed IT Patent 102023000006180, March 2023.
4. **T. Cucinotta**, D. Cherubini, E. Jul. "*Secure Data Processing*," Filed US Patent 14/405894. December 2014.
5. **T. Cucinotta**, D. Cherubini, E. Jul. "*Secure Data Processing*," Filed US Patent 14/399372. November 2014.
6. **T. Cucinotta**, A. Meroni, V. Hilt. "*State Migration for Elastic Virtualized Components*," Filed US Patent 14/338502. July 2014.
7. **T. Cucinotta**. "Method for Managing User Requests in a Distributed Computing Environment and Computer Program Product," Filed EU Patent 14305652. April 2014.
8. **T. Cucinotta**. "*Method For Virtual Machine Instantiation, Scalable Computing System, Virtual Machine And Computer Program Product*," Filed EU Patent 14305558. April 2014.
9. **T. Cucinotta**, I. Bedini. "*Method, Processing Framework, Aggregator And Computer Program Product For Processing Data*," Filed EU Patent 13360033. October 2013.
10. **T. Cucinotta**. "*Method and System for Graphical User Interface Layout Generation, Computer Program Product*," Filed EU Patent 13360015. August 2013.
11. **T. Cucinotta**, A. Sala. "*Methods and Devices for Protecting Private Data*," Filed US Patent 13/944964. July 2013.
12. **T. Cucinotta**, "*Methods and Devices for Controlling Access to Distributed Resources*," Filed US Patent 13/926832. June 2013.
13. **T. Cucinotta**, I. Bedini. "*Method for Data Processing, Element to Process Data, Method for Monitoring Activity and Computer Program Product*," Filed EU Patent 13360010. May 2013.
14. **T. Cucinotta**. "*Scheduling*," Filed EU Patent 20130305397. March 2013.
15. I. Bedini, **T. Cucinotta**, A. Sala, B. Theeten. "*Systems And Methods For Self-Adaptive Distributed Systems*," Filed US Patent 13/853533. March 2013.
16. **T. Cucinotta**, D. Cherubini, E. Jul. "*Collaborative Uses of a Cloud Computing Confidential Domain of Execution*," Filed US Patent 13/622007. September 2012.
17. D. Cherubini, **T. Cucinotta**. "*System Control*," Filed EU Patent 20120360068. September 2012, and Filed US Patent 14/423967
18. **T. Cucinotta**, D. Cherubini, E. Jul. "*Secure Data Processing*." Filed EU Patent 20120360044. June 2012
19. **T. Cucinotta**, "*Task Scheduling*." Filed EU Patent 20120360037. May 2012

Publications

ARTICLES IN INTERNATIONAL PEER-REVIEWED SCIENTIFIC JOURNALS

1. L. Pannocchi, S. Lahiri, S. Fichera, A. Artale, **T. Cucinotta**. "*Datacenter Optimization Methods for Softwarized Network Services*," Elsevier Journal of Systems Architecture (JSA), Vol. 156, November 2024
2. F. Galli, K. Jung, S. Biswas, C. Palamidessi, **T. Cucinotta**. "*Advancing Personalized Federated Learning: Group Privacy, Fairness, and Beyond*," Springer Nature Computer Science, September 2023
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ARTICLES IN PROCEEDINGS OF INTERNATIONAL PEER-REVIEWED CONFERENCES AND WORKSHOPS

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65. **T. Cucinotta**, D. Lugones, D. Cherubini, K. Oberle. "Brokering SLAs for end-to-end QoS in Cloud Computing," in Proceedings of the 4th International Conference on Cloud Computing and Services Science (CLOSER 2014), 3-5 April 2014, Barcelona, Spain
66. **T. Cucinotta**, D. Cherubini, E. Jul. "Confidential Execution of Cloud Services," in Proceedings of the 4th International Conference on Cloud Computing and Services Science (CLOSER 2014), 3-5 April 2014, Barcelona, Spain
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69. **T. Cucinotta**. "*Priority Inheritance on Condition Variables*," in Proceedings of the 9th International Workshop on Operating Systems Platforms for Embedded Real-Time applications (OSPERT 2013), July 9th, 2013, Paris, France
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74. **T. Cucinotta**, G. Anastasi. "*A Heuristic for Optimum Allocation of Real-Time Service Workflows*," in Proceedings of the IEEE International Conference on Service-Oriented Computing and Applications (SOCA 2011), Irvine, CA, December 2011
75. L. Abeni and **T. Cucinotta**, "*Efficient Virtualisation of Real-Time Activities*," in Proceedings of the IEEE International Workshop on Real-Time Service-Oriented Architecture and Applications (RTSOAA 2011), December 12-14 2011, Irvine, CA
76. G. F. Anastasi, **T. Cucinotta**, G. Lipari, M. Garcia-Valls, "*A QoS Registry for Adaptive Real-Time Service-Oriented Applications*," in Proceedings of the IEEE International Workshop on Real-Time Service-Oriented Architecture and Applications (RTSOAA 2011), December 12-14 2011, Irvine, CA
77. **T. Cucinotta** and V. Subramanian. "*Characterization and analysis of pipelined applications on the Intel SCC*," 4th MARC Symposium, Potsdam, Germany, December 2011
78. **T. Cucinotta**. "*Optimum Scalability Point for Parallelisable Real-Time Components*," in Proceedings of the International Workshop on Synthesis and Optimization Methods for Real-time and Embedded Systems (SOMRES 2011), co-located with the 32nd IEEE Real-Time Systems Symposium (RTSS 2011), Vienna, Austria, November 29 - December, 2011
79. **T. Cucinotta**, S. Gogouvitis, K. Konstanteli. "*SLAs in Virtualized Cloud Computing Infrastructures with QoS Assurance*," in Proceedings of the International Workshop on eContracting in the Clouds, co-located with the eChallenges 2011 Conference, Florence, Italy, October 2011
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81. J. Lelli, G. Lipari, D. Faggioli, **T. Cucinotta**, "*An efficient and scalable implementation of global EDF in Linux*," in Proc. of the 7th International Workshop on Operating Systems Platforms for Embedded Real-Time Applications (OSPERT 2011), Porto, Portugal, July 2011
82. **T. Cucinotta**, D. Faggioli, G. Bagnoli, "*Low-Latency Audio on Linux by Means of Real-Time Scheduling*," in Proceedings of the Linux Audio Conference (LAC 2011), Maynooth, Ireland, May 2011
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 87. **T. Cucinotta**, D. Giani, D. Faggioli and Fabio Checconi, "Providing Performance Guarantees to Virtual Machines using Real-Time Scheduling," in Proceedings of the 5th Workshop on Virtualization and High-Performance Cloud Computing (VHPC 2010), Ischia (Naples), Italy, August 2010
 88. **T. Cucinotta**, D. Faggioli, "An Exception Based Approach to Timing Constraints Violations in Real-Time and Multimedia Applications," in Proceedings of the IEEE Symposium on Industrial Embedded Systems (SIES 2010), Trento, Italy, July 2010
 89. D. Faggioli, G. Lipari, **T. Cucinotta**, "The Multiprocessor BandWidth Inheritance Protocol," in Proceedings of the 22nd Euromicro Conference on Real-Time Systems (ECRTS 2010), Bruxelles, Belgium, July 2010
 90. **T. Cucinotta**, F. Checconi, L. Abeni, L. Palopoli, "Self-tuning Schedulers for Legacy Real-Time Applications," in Proceedings of the 5th ACM European Conference on Computer Systems (EuroSys 2010), Paris, France, April 2010
 91. **T. Cucinotta**, Konstanteli K., Varvarigou T., "Advance Reservations for Distributed Real-Time Workflows with Probabilistic Service Guarantees," in Proceedings of the IEEE International Conference on Service-Oriented Computing and Applications (SOCA 2009), Taipei, Taiwan, December 2009
 92. **T. Cucinotta**, L. Abeni, L. Palopoli, F. Checconi, "The Wizard of OS: a Heartbeat for Legacy Multimedia Applications," in Proceedings of the 7th IEEE Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia 2009), Grenoble, October 2009
 93. **T. Cucinotta**, G. Lipari, L. Palopoli, L. Abeni, Santos R., "Multi-level feedback control for Quality of Service Management," in Proc. of the 14th IEEE International Conference on Emerging Technologies and Factory Automation, Palma de Mallorca (ETF A 2009), Spain, September 2009
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 95. **T. Cucinotta**, G. Anastasi, L. Abeni, "Respecting temporal constraints in virtualised services," in Proc. of the 2nd IEEE International Workshop on Real-Time Service-Oriented Architecture and Applications (RTSOAA 2009), Seattle, Washington, July 2009
 96. K. Konstanteli, D. Kyriazis, T. Varvarigou, **T. Cucinotta**, G. Anastasi, "Real-time guarantees in flexible advance reservations," in Proc. of the 2nd IEEE International Workshop on Real-Time Service-Oriented Architecture and Applications (RTSOAA 2009), Seattle, Washington, July 2009
 97. F. Checconi, **T. Cucinotta**, D. Faggioli, G. Lipari, "Hierarchical Multiprocessor CPU Reservations for the Linux Kernel," in Proc. of the 5th International Workshop on Operating Systems Platforms for Embedded Real-Time Applications (OSPRT 2009), Dublin, Ireland, June 2009
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Operating Systems Platforms for Embedded Real-Time Applications (OSPERT 2008), Prague, Czech Republic, July, 2008

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107. **T. Cucinotta**, D. Corcoran, M. Di Natale, "A protocol for programmable smart cards", Trust and Privacy in Digital Business Workshop, Prague, Czech Republic. In Proc. of the 14th International Workshop on Database and Expert Systems Applications (DEXA 2003), September 2003.
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111. **T. Cucinotta**, L. Palopoli, L. Marzario, "Stochastic feedback-based control of QoS in soft real-time systems", in Proceedings of the 43rd IEEE Conference on Decision and Control (CDC 2004), Bahamas, December 2004
112. L. Palopoli, **T. Cucinotta**, A. Bicchi, "Quality of service control for soft real-time applications", in Proc. of the 42nd IEEE Conference on Decision and Control (CDC 2003), Hawaii, USA, Dec. 2003

ARTICLES IN PROCEEDINGS OF ITALIAN PEER-REVIEWED CONFERENCES AND WORKSHOPS

113. M. Di Natale, **T. Cucinotta**, P. Ancilotti, "Lo sviluppo di una architettura modulare open-source per i servizi della PA: considerazioni tecniche e organizzative", in proceedings of SALPA: Sapere Aperto e Libero nella Pubblica Amministrazione, Marzo 2004, Pisa

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39. **T. Cucinotta**. "Cybersecurity (in Distributed Computing Systems)," Encyclopedia of Law and Data Science, pp. 92-97, ed. G. Comandé, Edward Elgar Publishing, February 2022. ISBN: 978-1-83910-458-9
40. L. Schubert L., S. Wesner, D. R. Bonilla, **T. Cucinotta**. "Autonomic Distribution and Adaptation," Programming Multi-core and Many-Core Computing Systems. Wiley Interscience. February 2017. ISBN: 978-0-470-93690-0
41. **T. Cucinotta**, G. Lipari, L. Schubert. "Operating System and Scheduling for Future Multi-core and Many-Core Platforms," Programming Multi-core and Many-Core Computing Systems. Wiley Interscience. February 2017. ISBN: 978-0-470-93690-0
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46. E. Oliveros, **T. Cucinotta**, S. C. Phillips, X. Yang, T. Voith, S. Middleton. “*Monitoring and Metering in the Cloud*,” Achieving Real-Time in Distributed Computing: From Grids to Clouds. IGI Global, July 2011. DOI: 10.4018/978-1-60960-827-9
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50. **T. Cucinotta**. “*Privacy nell'era dei big-data e il cittadino «privato»*,” capitolo all'interno del volume “Manuale per il trattamento dei dati personali,” a cura di G. Comandè e G. Malgieri, pp. 127-129, Il Sole 24 Ore, Marzo 2018. ISBN: 9788832491326
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52. **T. Cucinotta**, “*Firma digitale e assicurazioni: aspetti tecnologici*”, L'economia digitale e il settore assicurativo, DEA Quaderni di Impresa Assicurativa, Giuffrè Editore, 2003

Software development in open-source projects

- ❑ **2022**: patches to [Gnuplot](#), [adding the cubic root function](#), and fixing a [bug in handling covariance fitting variables](#)
- ❑ **2020-2023**: creator of the [distwalk](#) distributed processing benchmark: <https://github.com/tomcucinotta/distwalk>
- ❑ **2017**: patches to [auto-connect ALSA midi inputs](#), both at start and at [runtime](#), in the fluidsynth software synthesizer
- ❑ **2017**: [bugfix in the real-time meter display](#) code and [speed-up of the audio processing pipeline](#) of MuseScore
- ❑ **2016**: contributed patches to the [mainline Linux kernel](#) to [speed-up heap operations](#) within SCHED_DEADLINE, [refactor the heap code](#) and [fix a wrap-around bug](#) in deadline comparisons
- ❑ **2007 to date**: active contributor to the LyX open-source project (C++): <http://www.lyx.org>
Developed advanced format-aware find/replace, XMPP-based chat, external material management, bugfixes
- ❑ **2008-2010**: IRMOS real-time scheduler for the Linux kernel (C): <http://lwn.net/Articles/398470/>
Contributed to the design of the main scheduler features
- ❑ **2012**: contributed to the MuseScore open-source music notation editor (C++): <http://www.musescore.org/>
Feature for automatic detection of repeating segments in scores and application of corresponding notation
- ❑ **2011**: contributed to the Jack2 open-source low-latency audio infrastructure (C++): <http://repo.or.cz/w/jack2.git>
Designed and contributed to the integration of Jack2 with the AQuoSA deadline-based scheduler on Linux
- ❑ **2011**: creator of the MCoreSim network-on-a-chip simulator (OMNeT++): <http://sourceforge.net/projects/mcoresim/>
- ❑ **2010**: contributed to the OWL open-source document management system (PHP)
Tiny patch for faster access to the external link feature
- ❑ **2009-2012**: Contributed to the RTSim real-time systems simulator (C++): <https://sourceforge.net/projects/rtsim/>
- ❑ **2009-2023**: Creator of the Open Macro Library (OML): <http://oml.sourceforge.net>, <https://github.com/tomcucinotta/oml>
- ❑ **2006-2010**: Adaptive Quality of Service Architecture (AQuoSA) for Linux kernel (C): <http://aquosa.sourceforge.net>
- ❑ **2006-2009**: Creator of the ARSim Adaptive Reservations simulator (C++): <http://gna.org/projects/arsim/>
- ❑ **2001**: MuscleCard, open-source smartcard middleware for Linux (JavaCard/C/C++): <http://www.musclecard.com>
- ❑ **2000-2006**: Creator of SmartSign: <http://smartsign.sourceforge.net>
- ❑ **2000-2001**: Designed/developed open-source registry for Public Administration (Python), in production for 6 years

- ❑ **2000:** Dienst digital library software (Perl): Design and implementation of an advanced document object model

Informal university assignments

- ❑ Semiformal design, using Unified Modeling Language (UML), of a *system for event based emulation of generic digital circuits*.
- ❑ Design and realization, using C++, of a command line *discrete event based emulator* for the PIC16C84 microcontroller.
- ❑ Design and realization, using C, of a simplified *transport level network protocol* (OSI terminology).
- ❑ Implementation, using Matlab, of the *Simplex algorithm* for the resolution of Linear Programming optimization problems.
- ❑ Design and realization, using Visual C++, of a *program for the automatic generation of a web page (HTML/Javascript)* supporting students in the selection of the study plan.

Computer science background

RESEARCH TOPICS WITH STATE-OF-THE-ART KNOWLEDGE

- ❑ Scheduling of soft real-time tasks and virtual machines for quality of service control
- ❑ Operating Systems for multi-core and many-core systems
- ❑ Secure processing architectures
- ❑ Protocols and architectures for smart-card interoperability
- ❑ Access control models: Role Based Access Control (RBAC) and its variants, Multi Level Security (MLS)
- ❑ Key management algorithms and protocols for secure data streaming
- ❑ Formal methods: Burrows, Abadi, Needham (BAN) logic of authentication and its variants

SECURITY-SPECIFIC STANDARDS, PROTOCOLS, LIBRARIES AND TOOLS

- ❑ PKCS standards, ISO 7816 standards, PCSC Standards, X.509, S/MIME, XML-Signature
- ❑ Secure Socket Layer (SSL) protocol, Secure SHell (SSH) protocol
- ❑ Detailed knowledge of cryptosystems: RSA, DSA, DES, Rijndael (AES), Elliptic Curve (EC)
- ❑ Biometrics recognition techniques, BioAPI, Biometrika FX2000 and FX3 SDK
- ❑ Microsoft CryptoAPI, Java Security Architecture (JSA) and API, JavaCard-2.x, Open Card Framework (OCF), OpenSSL, OpenSSH, Pretty Good Privacy (PGP), ModSSL for Apache
- ❑ Schlumberger Cyberflex Access Toolkit, CompEd DigitalSign and DigitalSign API

EMBEDDED SYSTEMS DEVELOPMENT AND DESIGN

- ❑ Z-World: Rabbit Core Module 3000, Dynamic C
- ❑ Texas Instruments: TMS320C6711, Code Composer Studio
- ❑ Altera: Stratix EP1S40 FPGA, Nios II CPU Core, Quartus II, SOPC Builder, Nios II IDE, ModelSim
- ❑ Verilog Hardware Description Language (Verilog HDL), VHDL

PROGRAMMING LANGUAGES & FRAMEWORKS

- ❑ C/C++, Java 1.x and 5.0, Design Patterns, OpenMP, MPI, Storm
- ❑ gcc, gcov, gdb, Valgrind, advanced knowledge of GNU make, autotools (autoconf/automake)
- ❑ Standard Template Library (STL), Boost library, OpenGL, DirectX
- ❑ Assembler Intel 80x86, Assembler Motorola 68000
- ❑ Unix Bourne Again Shell (BASH) scripting, Regular Expressions
- ❑ Microsoft Visual C++ v5.0, Microsoft Visual Basic, Rational Rose '98, Kdevelop, Eclipse
- ❑ Microsoft Windows API, Microsoft Foundation Classes (MFC)
- ❑ X Toolkit, Motif, Qt, KDE, Gtk, WxWindows
- ❑ JavaScript, JScript, Perl, Php, Python, Visual Basic and VBA, VBScript, Pascal, Basic
- ❑ Octave, Gnuplot, Matlab, GLPK, Symphony
- ❑ Intel Integrated Performance Primitives (IPP) library, SIP, Metaswitch Clearwater

OTHER LANGUAGES

- ❑ XML, Dynamic HTML, Cascaded Style Sheets (CSS), LaTeX, Unified Modeling Language (UML) Notation
- ❑ Structured Query Language (SQL), CORBA Interface Description Language (IDL)
- ❑ Ontology Web Language (OWL), Protégé Ontology Editor

OPERATING SYSTEMS

- Linux administration, kernel tuning and hacking (driver and scheduler development). Experienced with Solaris
- Android OS and programming
- Microsoft Windows 95/98/NT/ME/2000/XP, MS DOS

VARIOUS

- Z Object Publishing Environment (Zope)
- Microsoft Office (and MS Office Automation), Microsoft Front Page
- Italian law on digital signatures: “Codice [...]” (D. Lgs. 82/2005), “Testo Unico [...]” (DPR 445/2000)
- European Directive 1999/93/CE: “Community Framework for Electronic Signatures”

Foreign languages

- Excellent knowledge of both spoken and written *English*.
- Basic knowledge of *German*.

Personal interests

- Computer Security, Smart Cards, Biometrics Identification
- Hardware architectures for cryptographic accelerators and 3D accelerators
- 3D graphics and rendering engines
- Audio signal processing algorithms, audio signal and voice synthesis and recognition
- Neural networks, Artificial Intelligence, semantics-based computing